| O.P.Code: 20EC0442 | R20 | H.T.No. | | | | | | | | | |
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**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR**

(AUTONOMOUS)

**B.Tech IV Year I Semester Regular Examinations February-2024**

**VLSI DESIGN**

(Electronics & Communication Engineering)

**Time: 3 Hours** **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

**UNIT-I**

| | | | | | |
|---|---|---|---|---|---|
| 1 | a | Summarize the evolution of microelectronics. | CO1 | L2 | 6M |
| | b | Explain working of the NMOS transistor. | CO1 | L2 | 6M |
| | | **OR** | | | |
| 2 | a | Define Metal Oxide Semiconductor VLSI Technology. | CO1 | L2 | 6M |
| | b | List the advantages and disadvantages of IC | CO1 | L1 | 6M |
| | | **UNIT-II** | | | |
| 3 | a | What are lambda-based design rules? Explain. | CO3 | L1 | 6M |
| | b | Illustrate design rules for wires and MOS transistors. | CO3 | L2 | 6M |
| | | **OR** | | | |
| 4 | a | Explain about Stick diagram with one example. | CO3 | L2 | 6M |
| | b | Sketch the layout diagram for 2-input CMOS NAND gate. | CO3 | L3 | 6M |
| | | **UNIT-III** | | | |
| 5 | a | Sketch 2 x 1 mux using transmission gates. | CO4 | L3 | 6M |
| | b | Explain the implementation of AOI using CMOS design style with neat sketches. | CO4 | L2 | 6M |
| | | **OR** | | | |
| 6 | a | What is switch logic? Explain with an example. | CO4 | L2 | 6M |
| | b | Explain about pass transistors logic with an example. | CO4 | L1 | 6M |
| | | **UNIT-IV** | | | |
| 7 | a | Explain different adder designs in sub circuit design with neat sketches. | CO6 | L2 | 6M |
| | b | Differentiate Comparator and Magnitude Comparator with example. | CO6 | L4 | 6M |
| | | **OR** | | | |
| 8 | | Explain the following logic circuit<br>(i) Parity Generator (ii) Comparator | CO6 | L2 | 12M |
| | | **UNIT-V** | | | |
| 9 | a | Explain in detail about standard cell design with suitable diagrams. | CO6 | L2 | 6M |
| | b | Give examples of various fault models available for VLSI testing. | CO5 | L2 | 6M |
| | | **OR** | | | |
| 10 | a | What is the need for testing? Explain about Fault simulation. | CO5 | L1 | 6M |
| | b | Give a logic circuit example in which stuck-at-1 fault and stuck-at-0 fault are indistinguishable. | CO5 | L2 | 6M |

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